REMARKS

Claims 1, 3-5, 8, and 10-13 are now pending in the application. By this paper, Claims 1, 11, and 13 have been amended and Claims 2, 6, 7, 9, and 14-17 have been cancelled without prejudice or disclaimer of the subject matter contained therein. The basis for these amendments can be found throughout the specification, claims, and drawings originally filed. No new matter has been added. The preceding amendments and the following remarks are believed to be fully responsive to the outstanding Office Action and are believed to place the application in condition for allowance.

The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3-5, 8, 10, 11, 12, stand rejected under 35 U.S.C. § 102(e) as being anticipated by Degani et al. (U.S. PG Pub#20020079568).

This rejection is respectfully traversed.

Independent Claim 1 calls for a semiconductor device including a first carrier substrate, a first semiconductor chip mounted face down on the first carrier substrate, a second semiconductor chip mounted face down on a reverse face of the first carrier substrate, a second carrier substrate, a third semiconductor chip mounted on the second carrier substrate, and protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first semiconductor chip. In addition, independent Claim 1 recites that the third semiconductor chip comprises a structure in which a plurality of chips are stacked.

Independent Claim 11 calls for an electronic device including a first carrier substrate, a first semiconductor chip mounted face down on at least one face of the first carrier substrate, a second carrier substrate, a second semiconductor chip mounted on the second carrier substrate, a third semiconductor chip mounted on a reverse face of the second carrier substrate, and protruding electrodes bonding the second carrier substrate to the first carrier substrate. In addition, independent Claim 11 recites that the third semiconductor chip comprises a structure in which a plurality of chips are stacked.

Independent Claim 12 calls for a semiconductor device including a carrier substrate, a first semiconductor chip mounted face down on the carrier substrate, a second semiconductor chip mounted face down on a reverse face of the carrier substrate, a third semiconductor chip on which re-arrangement wiring line layers are formed on surfaces where electrode pads are formed, and protruding electrodes connecting the third semiconductor chip to the carrier substrate so that the third semiconductor chip is held above the first semiconductor chip.

In this manner, the present invention discloses a carrier substrate (21) having semiconductor chips (23a and 23b) mounted on two faces of the carrier substrate (21) and a carrier substrate (31) having semiconductor chips (33a and 33b) mounted thereon. See Specification at pg. 11, Paragraph [0053], pg. 13, Paragraph [0057], and FIG. 1. The semiconductor chips (33a and 33b) are stacked on the carrier substrate (31) such that the semiconductor chip (33a) is disposed generally between the carrier substrate (31) and the semiconductor chip (33b). See FIG. 1. The carrier substrate (31) is "held above" the carrier substrate (21) by protruding electrodes (36) to allow the semiconductor chips (33a and 33b) to be stacked on a first face of the carrier substrate

(31) while maintaining a space between a second face of the carrier substrate (31) and the semiconductor chip (25a). See Specification at pg. 13, Paragraph [0058] and FIG. 1. Such a relationship makes it possible to stack differently packaged semiconductor chips (33a and 33b) on semiconductor chips (23a and 23b) while suppressing warpage of the carrier substrate (21). See Specification at pg. 13, Paragraph [0059].

Degani fails to teach a first carrier substrate having semiconductor chips mounted on two faces thereof and a second carrier substrate having semiconductor chips stacked thereon. Furthermore, Degani fails to teach positioning the second carrier substrate and stacked semiconductor chips relative to the first carrier substrate and first semiconductor chips such that the second carrier substrate and stacked semiconductor chips are held above the first carrier substrate and first semiconductor chips.

Rather, Degani teaches a first carrier substrate (26) and a second carrier substrate (22) connected to the first carrier substrate by a series of solder balls (27). See Degani at pg. 2, Paragraph [0024] and FIG. 3. IC chips (23, 31) are mounted on two sides of the second carrier substrate using solder bumps (32). See Degani at pg. 2, Paragraph [0026] and FIG. 3.

In this manner, Degani fails to teach a first carrier substrate having first semiconductor chips mounted on two sides thereof and a second carrier substrate having second semiconductor chips stacked thereon. Furthermore, Degani fails to teach positioning the second carrier substrate and stacked second semiconductor chips such that the second carrier substrate and stacked second semiconductor chips are "held above" the first carrier substrate and the first semiconductor chips. Applicant

respectfully submits that even if the Examiner characterizes Degani as teaching a first carrier substrate (22) having IC chips (23, 31) mounted on two sides thereof, that Degani fails to teach mounting a second substrate above the first carrier substrate such that the second carrier substrate is "held above" the first carrier substrate and further fails to teach stacking semiconductor chips on the second carrier substrate such that the stacked semiconductor chips are similarly held above the first carrier substrate.

Because Degani fails to teach a first carrier substrate having semiconductor chips mounted on two faces thereof and a second carrier substrate having semiconductor chips stacked thereon, and further, because Degani fails to teach positioning the second carrier substrate and stacked semiconductor chips relative to the first carrier substrate and first semiconductor chips such that the second carrier substrate and stacked semiconductor chips are held above the first carrier substrate and first semiconductor chips, Applicant respectfully submits that Degani fails to teach each and every element of the present invention. Accordingly, Applicant respectfully submits that independent Claims 1 and 11-12, as well as Claims 3-5, 8, and 10, respectively dependent therefrom, are in condition for allowance. Therefore, reconsideration and withdrawal of the rejection is respectfully requested.

Claim 13 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Akram et al. (U.S. PG Pub#20010015488).

This rejection is respectfully traversed.

Independent Claim 13 calls for an electronic device including a first carrier substrate, a first electronic part mounted on the first carrier substrate, a second electronic part mounted on a reverse face of the first carrier substrate, a second carrier

substrate, a third electronic part mounted on the second carrier substrate, protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first electronic part, and a sealant for sealing the third electronic part. In addition, independent Claim 13 recites that the third semiconductor chip comprises a structure in which a plurality of chips are stacked.

As discussed above, the present invention discloses a carrier substrate (21) having semiconductor chips (23a and 23b) mounted on two faces of the carrier substrate (21) and a carrier substrate (31) having semiconductor chips (33a and 33b) mounted thereon. See Specification at pg. 11, Paragraph [0053], pg. 13, Paragraph [0057], and FIG. 1. The semiconductor chips (33a and 33b) are stacked on the carrier substrate (31) such that the semiconductor chip (33a) is disposed generally between the carrier substrate (31) and the semiconductor chip (33b). See FIG. 1.

Akram fails to teach a first carrier substrate having semiconductor chips mounted on two faces thereof and a second carrier substrate having semiconductor chips stacked thereon. Rather, Akram teaches a base substrate (102) and first and second stacked substrates (116, 140). See Akram at pg. 3, Paragraphs [0033-0035], pg. 4, Paragraph [0036], and FIG. 1. The first stacked substrate has a semiconductor dice (128) mounted thereon while the second stacked substrate has a pair of semiconductor die (150, 162) mounted on two sides thereof. See Akram at pg. 3, Paragraph [0035], pg. 3, Paragraph [0037], and FIG. 1.

Applicant respectfully submits that even if the Examiner characterizes the second substrate (140) as including a pair of semiconductor devices that Akram fails to teach a

carrier substrate held *above* the second substrate having semiconductor devices stacked thereon.

Because Akram fails to teach a first carrier substrate having semiconductor chips mounted on two faces thereof and a second carrier substrate having semiconductor chips stacked thereon, Applicant respectfully submits that Akram fails to teach each and every element of the present invention. Accordingly, Applicant respectfully submits that independent Claim 13 is in condition for allowance. Therefore, reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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